REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-13 are presently pending in this application. Claims 1 and 4 are amended by the present amendment. Support for the subject matter amended to Claims 1 and 4 is found in Applicants' Figures 1, 6 and 14-17, for example. No new matter is added.

In the outstanding Office Action, Claims 1, 2 and 4-7 were rejected under 35 U.S.C. § 102(e) as anticipated by Takeuchi et al. (U.S. Patent 6,366,490, herein "Takeuchi"); and Claims 3 and 8-13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Takeuchi.

Initially, the specification is amended for clarification. No new matter is added.

Before treating the outstanding art based rejections, it is believed that a brief review of a conventional ferroelectric memory and the present invention directed to a semiconductor integrated circuit device (i.e. a ferroelectric memory) may be helpful.

In a conventional ferroelectric memory, a plate line driver is provided for each plate line (i.e. one plate line driver is necessary for every two-row memory cell blocks). Accordingly, the plate line drivers occupy a large area in a semiconductor chip, rendering a reduction in size of the semiconductor chip difficult (see also the specification at page 2, lines 6-14, and at page 18, line 25 to page 19, line 1, for example).

According to features of the present invention as set forth in Claim 1, since one plate line driver is provided to a plurality of plate lines (i.e. the plate line driver is shared by the plurality of plate lines, or one plate line driver is provided for every four-row memory cell blocks), a number of plate line drivers can be reduced. Therefore, it becomes possible to reduce the size of the semiconductor chip (see also the specification at page 19, lines 2-14, for example).

Turning to the rejection, Claims 1, 2 and 4-7 were rejected under 35 U.S.C. § 102(e) as anticipated by Takeuchi. Applicants respectfully submit that the amendments to Claims 1 and 4 overcome the rejection for the following reasons.

In a non-limiting example, as set forth in Claim 1, Figure 1 illustrates plate lines (i.e. PL0, /PL0, PL1, /PL1) extending along a direction perpendicular to bit lines (i.e. BL0, /BL0, BL1, /BL1), and memory cell blocks (i.e. BLK00 and BLK02), which are connected to a plate line (i.e. PL0), connected to different sense amplifiers 40 (i.e. BLK00 connected to the left sense amplifier, and BLK02 connected to the right sense amplifier). Further, a plate line driver 60-1 is provided to the plate lines (i.e. PL0 and PL1). Claim 4 includes similar features.

Takeuchi discloses a structure (i.e. Figures 1 and 2) including plate lines PL formed along the same direction as bit lines BL, BBL, and memory cell blocks 3, which are connected to a plate line PL, connected to one sense amplifier 5. Further, a plate line driver 11 is provided to each plate line PL. In contrast to Takeuchi, as discussed above, the claimed "plate lines" extend in a direction perpendicular to the claimed "bit lines," the claimed "memory cell blocks," connected to a plate line, are connected to different sense amplifiers, and the claimed "plate line driver" is provided to a plurality of plate lines. More specifically, Takeuchi fails to disclose or suggest "... plate lines ... the plate lines extending along a second direction perpendicular to the first direction, and the memory cell blocks connected to one of the plate lines being connected to different ones of the sense amplifiers ... a plate line driver to which a plurality of the plate lines are connected and which applies a potential to the plate lines" as recited in amended Claim 1.

Further, in Takeuchi, since plate lines and bit lines are formed parallel to each other, the amount of wiring capacitance becomes large. Thus, a large-size plate line driver becomes necessary to accommodate an application of a large amount of load. Therefore, Takeuchi's

structure suffers from the problems of the conventional ferroelectric memory discussed above.

Accordingly, Applicants respectfully submit that Claims 1 and 4 are not anticipated by Takeuchi. In addition, Claims 2, 3 and 5-13 should be allowed, among other reasons, as depending from one of Claims 1 and 4, which should be allowed as just explained. Therefore, Applicants respectfully request that the anticipation of Claims 1, 2 and 4-7 under 35 U.S.C. § 102(e) be withdrawn.

Finally, with regard to Claims 2, 3, 7, 12 and 13, Applicants respectfully submit that the structure provided by the features of these claims has benefits in that the amount of load applied to a plate line driver would not become large even if a large number of plate lines share the plate line driver. Nowhere in Takeuchi is a suggestion or disclosure of such features, and Claims 2, 3, 7, 12 and 13 are believed to be non-obvious and patentable over Takeuchi and the above-noted benefits provided by the structure of Claims 2, 3, 7, 12 and 13 are not obviated by Takeuchi.

Consequently, in light of the above discussion, and in view of the present amendment, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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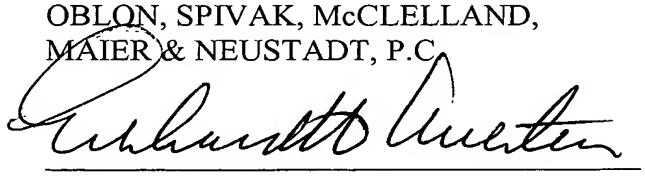

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